## 19.6 A Micropower Chopper-Stabilized Operational Amplifier using a SC Notch Filter with Synchronous Integration inside the Continuous-Time Signal Path

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Modern chopper and autozero opamps have significantly reduced or virtually eliminated switching noise. Different techniques are used and each has tradeoffs involving input-referred noise ($e_n$) and quiescent supply current ($I_q$). The inherent tradeoffs for chopper and autozero topologies are known (1). Choppers maintain the broadband noise characteristics of their input stage, but shift their input offset up to the chopping frequency ($f_s$) creating large ripple at the output. Autozero topologies do not shift their input offset to their autozero frequency ($f_s$) like choppers, but suffer from aliasing or folding back of their broadband noise spectrum sampled during their zeroing cycle to increase the overall input-referred noise. It can be shown for an ideal input stage that $e_n^2$ is inversely proportional to $I_q$, requiring autozero topologies to significantly increase $I_q$ in order to achieve the desired noise levels after noise folding [2, 3]. This fact makes it very desirable to use a chopper in micropower applications and find some way to limit the chopper ripple at $f_s$. Previous work has shown some improvement by employing both autozeroing and chopping, but that solution is not optimum for micropower applications [4].

We describe a chopper-stabilized opamp using a switched-capacitor notch filter with synchronous integration inside the continuous-time signal path to reduce chopping noise to well below the total rms noise. The opamp maintains the benefits of chopping while notching the ripple at $f_s$. The improvement is accomplished without an increase in $I_q$, making it suitable for micropower applications.

Figure 19.6.1 shows a 3-stage amplifier with multipath nested Miller compensation [5]. This topology can be thought of as a high-gain 3-stage opamp comprising $g_{m1}$, $g_{m2}$, and $g_{m3}$, in parallel with a wider bandwidth 2-stage opamp comprising $g_{m4}$ and $g_{m3}$. DC precision is determined by the input stage $g_{m1}$ in the high-gain path, while high-frequency response and phase margin are dominated by the 2-stage path. Proper selection of $g_m$'s and compensation can maintain the bandwidth and settling characteristics of a 2-stage Miller-compensated opamp with minimal increase in $I_q$, thereby achieving a good GBW/$I_q$ relationship. Figure 19.6.2 shows chopper stabilization added to the input stage ($g_{m1}$) in the dc path. The chopping significantly reduces offset, drift, and flicker noise, but shifts the $g_{m1}$ offset to $f_s$ as expected, and creates a large output ripple. Figure 19.6.4 shows the translation of a 10mV offset in $g_{m1}$ to a 75mV output ripple at $f_s$ with an opamp gain of 10. This ripple can be eliminated using the circuit shown in Fig. 19.6.3, which integrates the output of $g_{m1}$ (synchronously with the chopping) before transferring the signal to the next stage, $g_{m2}$. We have built this circuit and describe it in more detail in the following.

Consider that a positive offset current flows from $g_{m1}$ during phase 1 and an equal and opposite negative offset current flows during phase 2 as a result of chopping its input offset voltage. This offset signal is nulled by integrating $^1/_2$ of the positive phase-1 offset current and $^1/_2$ of the negative phase-2 offset current onto C5 during phase 3 for a net charge of 0 before transferring it to $g_{m2}$ during phase 4. In phase 4, C6 is used to integrate the equal and opposite offset currents from chopping $g_{m1}$ for a net charge of 0 as well. C5 and C6 work in tandem during phase 3 and phase 4 to integrate and transfer the chopped offset current from $g_{m1}$ as shown by the timing diagram. Referring to Fig. 19.6.4 again, a 500× reduction in ripple is shown. Simulation results are used here because the low-level ripple is buried well below the total rms noise and is not seen on an oscilloscope. Figure 19.6.5 shows measured noise spectra with $f_s$ visible just above the noise floor. While the deep notch created by the filter is desirable for removing the ripple, it may also filter the signal to some degree. A delay is created by the integrate-and-transfer action, which will affect the circuit differently depending on how the compensation capacitors are connected. Notice that C2 and C3 have been split; the "b" portion returns to the filter input and the "a" portion returns to the filter output. Returning compensation to the filter input through C2b has the advantage of maintaining a continuous-time path for the normal signal, but the potential for local-loop instability arises due to the delay of the switched-capacitor filter being in the local feedback path through C2b. Returning the compensation to the filter output though C2a provides a direct feedback path for local-loop stability, but now the normal signal is delayed by the switched-capacitor filter and may distort the large-signal response. This design returns most of the compensation, 6pF, to the filter input to maintain good continuous-time characteristics, and 1pF is returned to the filter output for local-loop stability. The complex compensation is responsible for a slight rise in the noise floor beyond 20kHz, which is visible in Fig. 19.6.5.

The measured noise spectral density of 55nV/√Hz was accurately predicted by SPICE simulation using SPECTRE RF's periodic steady-state and periodic noise analyses. Low-frequency measurements of 1.2$\mu V_{pp}$ over 0.1 to 10Hz demonstrate that $e_n$is essentially flat to dc. General characteristics include rail-to-rail input and output operating with supplies of 1.8 to 5.5V over -40 to 125°C. The quiescent current $I_q$ is 15μA, the input offset is 2μV with 0.02μV/°C temperature dependence, the GBW is 350kHz, and the chopping frequency is 125kHz. Figure 19.6.6 compares this work to other chopper and autozero opamps with favorable figure of merits for both $e_n^2 \times I_q$ and GBW/$I_q$ demonstrating its utility for micropower and/or low-noise applications. The circuit uses 0.7mm$^2$ on a 0.6μm mixed-signal CMOS process and the micrograph is shown in Fig. 19.6.7.

*Acknowledgement:*
The authors thank the High Performance Linear IC Layout group at Texas Instruments and specifically John Graner for attention to critical matching and routing, parasitic extraction results, and symmetry. This and similar IC layouts have demonstrated it is possible to match silicon with simulation results for these types of circuits.

*References:*
[1] C. C. Enz and G. C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proc. of the IEEE*, vol. 84, no.9, pp1320-1324, Sept., 1996.
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[3] Texas Instruments Inc., "OPA335 data sheet," 2002.
[4] A. T. K. Tang, "A 3μV-Offset Operational Amplifier with 20nV/√Hz Input Noise PSD at DC Employing both Chopping and Autozeroing," *ISSCC Dig. Tech. Papers*, pp.386-387, Feb., 2002.
[5] J. Huijsing, "Operational Amplifiers Theory and Design," Kluwer Academic Publishers, 2001.

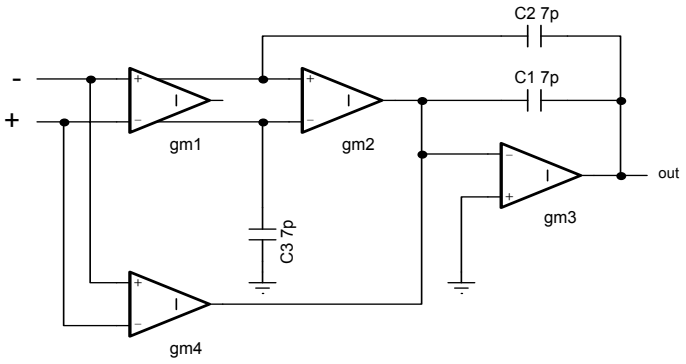



Figure 19.6.1: 3-stage amplifier with multipath nested Miller compensation.

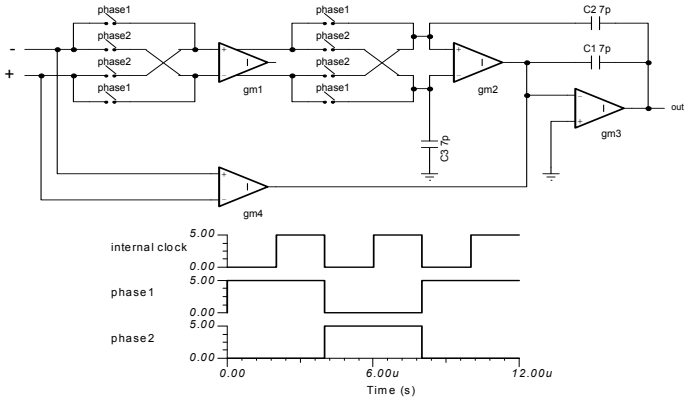
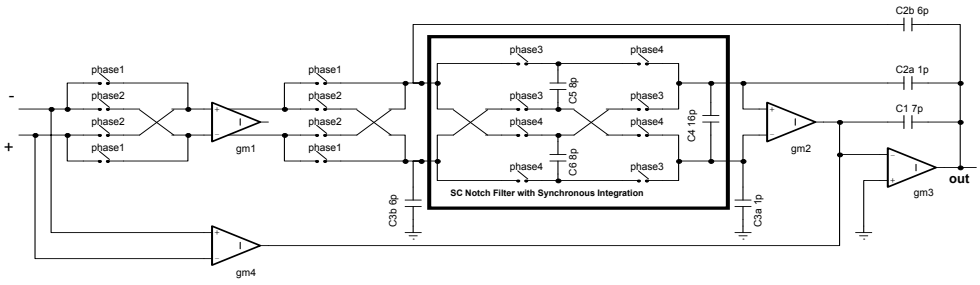



Figure 19.6.2: Chopping added to the input stage.



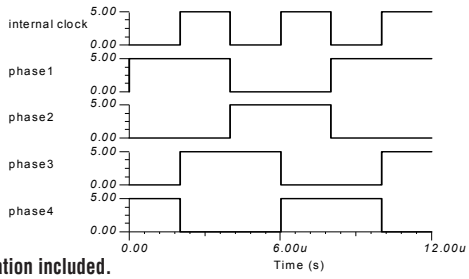




Figure 19.6.3: SC notch filter with synchronous integration included.

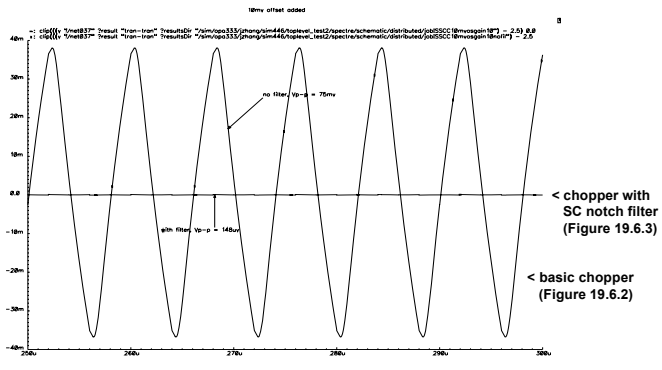



Figure 19.6.4: Transient simulation showing 500X less ripple; opamp gain G=10.

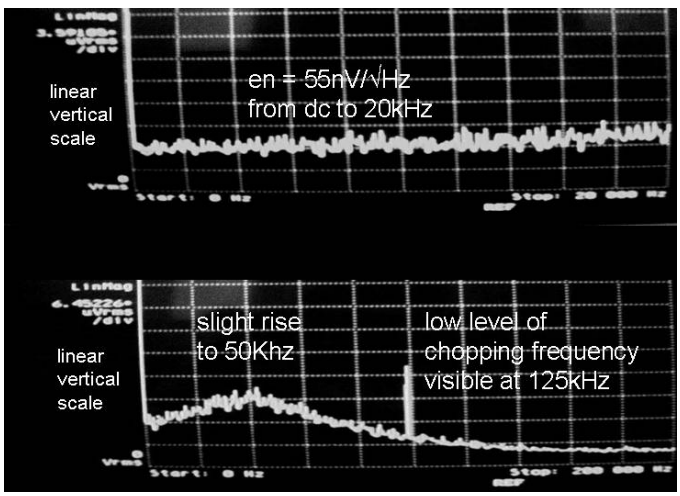



Figure 19.6.5: DC to 20kHz and 200kHz noise spectra; opamp gain G=10.

*Continued on Page 658*

| | This work | [2] | [3] | [4] |
|---|---|---|---|---|
| Year released/published | 2006 | 2004 | 2002 | 2002 |
| Chopping frequency | 125kHz | | | 15kHz |
| Autozero frequency | | 1kHz | 10kHz | 7.5kHz |
| Offset voltage (mean + std) | 2μV | 1μV | 1μV | 3μV |
| Input bias current | 70pA | 1pA | 70pA | 40pA |
| Gain Bandwidth, GBW | 350kHz | 500kHz | 2MHz | 2.5MHz |
| Input noise, en | 55nV/√Hz | 85nV/√Hz | 55nV/√Hz | 20nV/√Hz |
| Supply current, Iq | 15μA | 140μA | 285μA | 800μA |
| $en^2$ x Iq ($nV^2$ x uA) Figure of merit | 45 | 1011 | 862 | 320 |
| GBW/Iq (kHz/uA) Figure of merit | 23 | 4 | 7 | 3 |

Figure 19.6.6: Comparison of chopper and autozero opamps.

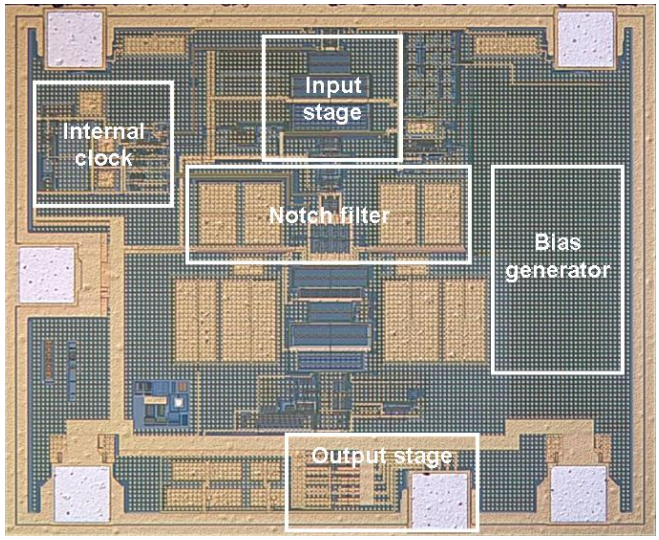



Figure 19.6.7: Chip micrograph.